Appendix I

Title:
Receive Buffer V2.1

1 Introduction

1.1 Overview

The Receive Buffer (RB) provides buffering of frame data and status between a Protocol Machine Receive (PMR) and Data Manage Unit Receive (DMUR). The PMR transfers data or status in 32 bit dword units to the RB which accumulates them in per channel buffers. When the count of dwords reaches a programmed burst size or a status word is transferred (status indicates end of frame or error), the RB transfers that channel's data to the DMUR as a block. The DMUR can then transfer data on the PCI bus in burst mode which results in more efficient bus usage.

The number of channels supported by the RB and the size of data buffers and burst event queues is fixed at synthesis time by VHDL package parameters. Buffers are built dynamically during operation from a free pool which should be dimensioned for the application dependent on number of channels and burst size. The throughput of the RB is naturally dependent on the speed of the PMR and DMUR but is ultimately limited by the RB's memory architecture (single port RAM and shared buffer pool). For long frames and large burst size, throughput could approach 3 clocks per double word but a more realistic limit for the average application is 4 clocks per dword.

The maximum aggregate serial bit rate is a function of system clock and the protocol frame size. Assuming a fully transparent protocol (no flags, bit stuffing), a 33MHz clock, and a conservative 5 clocks per dword results in 32 x 33/5 = 211 Mbit/second aggregate.

Features including performance, power usage, number of gates, area

- Buffers frame data and status per channel from a free pool common to all channels
- Per channel burst trigger. User specified (1, 4, 8, 16, 32, or 64 dwords) threshold
- Built In Self Test of RAM (BIST)
- system clock up to 66 MHz
- number of gates:
- area:
- power consumption:
- scan path

1.2 System Integration and Application

The RB interfaces are:

- configuration and control (Simplified Microprocessor Interface or SMIF) register oriented with separate read/write strobes per register
- Protocol Machine Receive (PMR) dword transfer. transfers blocked by flag when RB buffers flag.
- Data Management Unit Receive (DMUR) block oriented transfer of up to 64 dwords.
- Interrupts for buffer supervision

RB provides supervision of the free buffers in the data pool and action queue pool. RB interrupts can be asserted when buffer pool counts fall below user programmable thresholds. This provides an overload indication for flow control mechanisms and/or traffic engineering.

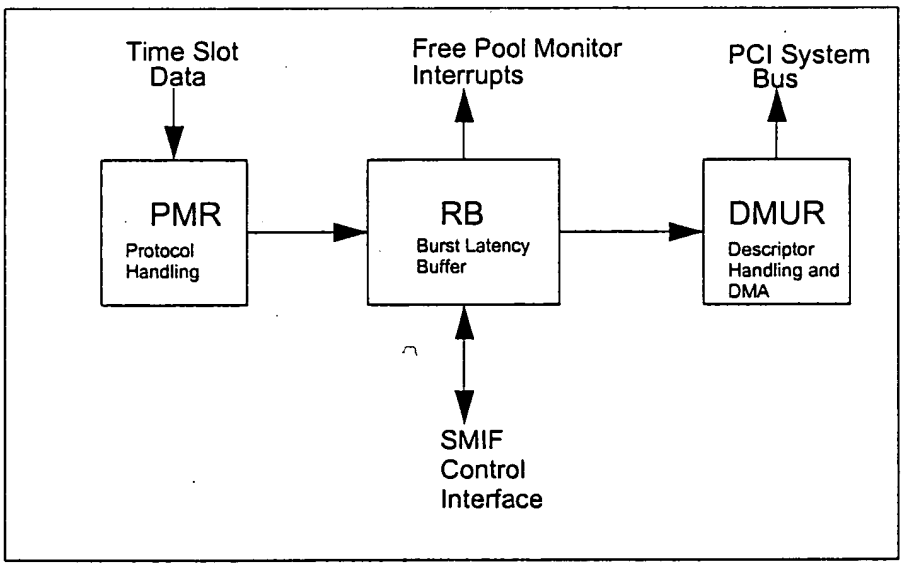

Figure 1
System Integration

1.3 Known Restrictions and Problems

2 Functional and Test Description

2.1 Block Diagram incl. Clocking Regions

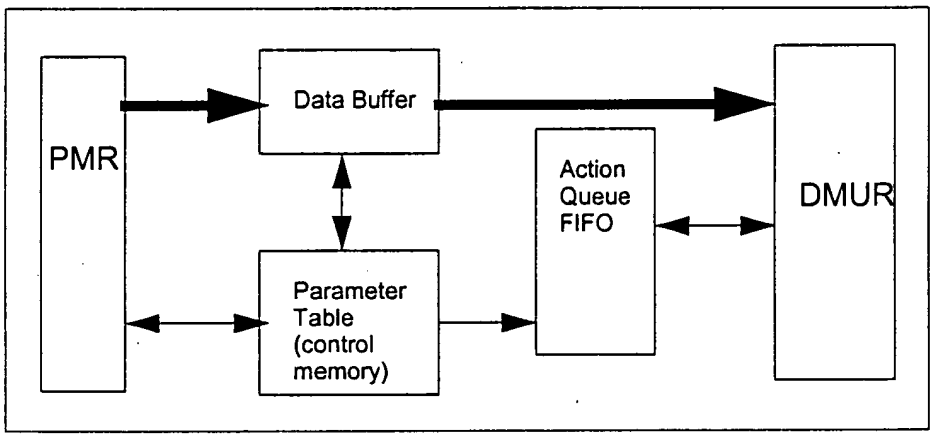

Figure 2
RB Block Diagram

2.2 Normal Operation Description

As shown in **Figure 2**, the main RB functions are realized in 3 blocks:

- Data Buffer (RBDB) for data buffers
- Parameter Table (RBPT) for control of individual channel queues
- Action Queue (RBAQ) for buffering of block requests for the DMUR

The PMR transfers data to the RB when:

- a 32 bit data word is filled with service data (data word) or
- end of frame or error condition is recognized (status word). a status word may contain from 0 to 3 octets of service data in addition to 1 octet of status.

PMR transfers a single dword by asserting a write strobe concurrently with:

1. data/status word (32 bit)
2. channel address (application dependent width)
3. control flag indicating the dword type (either service data or status+service data),
4. count of service data octets (only used if status word)
5. flag indicating if data currently stored in the RB for the channel should be discarded.

The channel number forms an index into the RB's parameter table which contains the channel's buffer control data. An element from a free buffer pool in RBDB is written with the new dword and linked to the channel's buffer chain. The free pool counts in RBDB and the read/write pointers and word count values in RBPT are updated.

When the channel's programmed burst threshold is reached or a status word is being transferred (end of frame or error), an entry is written to the RB Action Queue (RBAQ). A FIFO entry identifies the channel number, count of words to be transferred, type of the last dword in the burst (data or status+data), and the count of service data octets in a status word. Note that only the last word of a block being transferred is allowed to be status. The data and/or status dwords remain in the RBDB until transferred to the DMUR channel. When the FIFO is not empty, RB asserts a service request to the DMUR controller which initiates the data transfer.

If either RBDB or RBAQ becomes full, RB generates a buffer overflow indication by setting the RB_PRFULL line high. PMR must suppress any new data transfers. PMR is responsible to report the overflow.

A buffer discard function is activated by asserting PRDISCARD during the transfer. This allows PMR to discard channel data being accumulated in RB but which has not yet been transferred to the action queue. This feature is useful when the Protocol Machine recognizes that a frame is errored (e.g. too short) and should not be transferred to the software input queue. A discard for a channel should only be requested if the number of blocks transferred to the RB since the last status word is less than the channel's burst length. RB does not verify this.

2.2.1 Receive Buffer Parameter Table (RBPT)

The RBPT RAM provides a control word per channel for buffer management:

- Channel burst threshold
- Count of dwords in buffer chain not already sent to action queue FIFO
- Pointers for start and end of buffer chain (RBDB read and write addresses)
- Channel buffer status (empty/not empty)

Empty flag	Pre-Burst Count PBCNT (PC)	RD Pointer (BA)	WR Pointer (BA)	BTC (BC)

Burst Threshold Codes (BTC) are application dependent and fixed at synthesis by a table of constants in a VHDL package. Typical application are expected to use between 8 and 16 codes but this is not fixed in the architecture.

The width of the address bus BA is dependent on number of words RBDBS in the RAM.

$2^{BA-1} < RBDBS <= 2^{BA}$

When the accumulated count of dwords reaches the burst threshold or a status/discrd word is received, the chain of dwords is transferred to the Action Queue FIFO. The Pre-Burst Count (PBCNT) is the count-1 of words in the chain before it is transferred to the FIFO.

2^{PC} = maximum supported burst length e.g. 6 bits will support 64 word burst length.

The parameter table is implemented in 2 separately addressable RAMs to allow the SMIF interface to update the BTC without waiting on PMR/DMUR access of the PT:

1. Burst Parameter Code (BC)

MaxNumChan rows X BC columns

2. Channel Buffer State (read and write pointers, pre-burst count, and buffer empty flag)

. MaxNumChan rows X (2BA+PC+1) columns

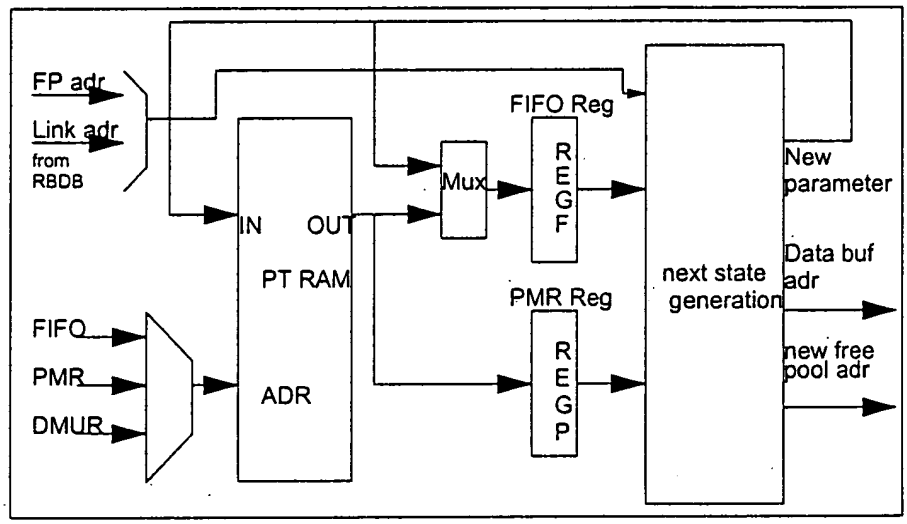

Figure 3
Receive Buffer Parameter Table (RBPT)

The pre-burst count PBCNT only has to count to 2^{PC}-1 for burst size 2^{PC}. The next dword transferred from PMR will generate an action request for the RBAQ FIFO and reset the PBCNT field to zero. The buffer empty flag is needed and cannot be derived from the PBCNT or read/write pointers because

1. PBCNT is zero following the transfer to the FIFO but dwords remain in the chain until the RBAQ FIFO has been serviced and

2. PBCNT=0 and WP=RP when burst length=1 or a single status word is transferred.

The RBPT is accessed by both the PMR and the DMUR service. PMR and DMUR (FIFO) service routines use separate output registers (REGR and REGF respectively) for the parameter table.

PMR service has the highest priority because it is essentially non-deferable.

PMR service when adding data to a buffer chain

A PMR request writes a single entry to RBDB. A read-modify-write of the channel's RBPT entry is performed using REGP. This can never be delayed by FIFO or slave FPI bus access.

FIFO service (RBAQ) when removing data from a buffer chain

A FIFO entry typically will read the parameter table, release multiple entries in the RBDB depending of burst length, and then write back the parameter table. The parameter table entry is copied to the REGF output register and updated during the burst. The RBPT ram is only updated at the end of the burst when it writes back REGF.

During the time a channel's RBPT entry is stored in the REGF, PMR service can access it to write data and update the channel's parameter table entry without delay. FIFO service is delayed during PMR service if this access is required. The PMR can not be deferred

2.2.2 RB Data Buffer (RBDB)

The RBDB Size (RBDBS) is sized according to:

- number of channels supported
- sum of channel bit rates
- burst threshold on bus
- maximum bus latency

An entry consists of a link field (BA bits wide) and data field (DB bits wide). The data and link fields are implemented in 2 physical RAMs to allow simultaneous read and write access of the data and link pointer fields at the same address.

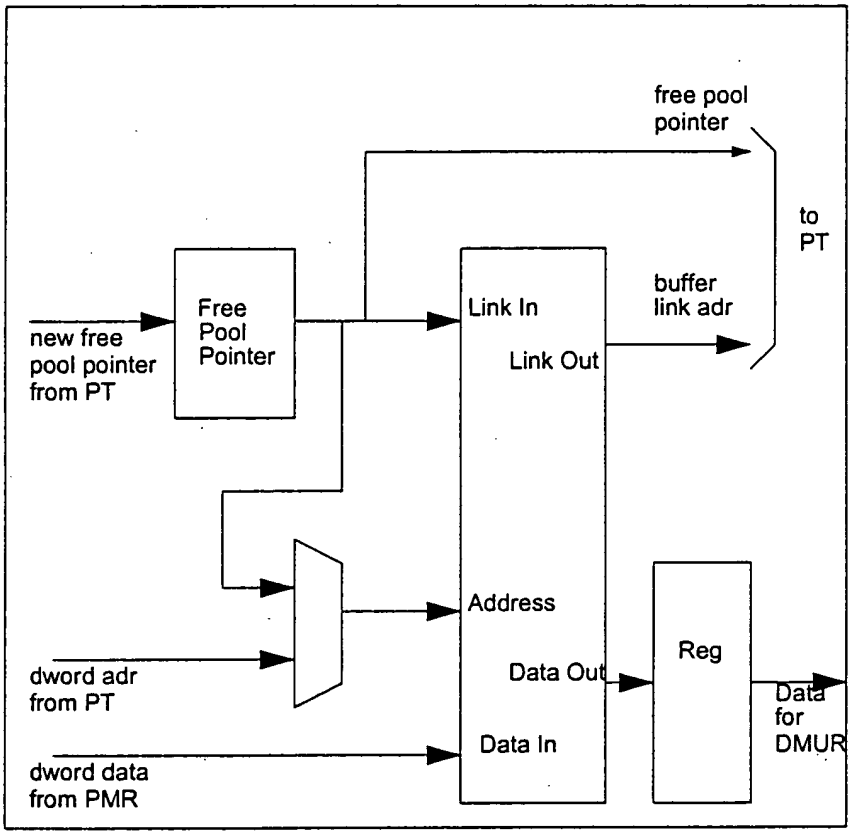

Figure 4
Structure of RB Data Buffer (RBDB)

2.2.3 RB Action Queue (RBAQ)

RBAQ is the FIFO which buffers the requests from RB to the DMUR Receive channel. An entry specifies:

- Channel Number
- Burst length
- Data type of last dword (protocol data or status)

- Number of service data octets in status dword

The data associated with a FIFO event remains in the RBDB until read by the DMUR. Because data can be delayed due to the higher priority PMR service, a ready signal is required at the DMUR interface for data transfers.

RBAQ size (RBAQS) is dimensioned according to:

- sum of channel bit rates
- minimum burst threshold on bus (1 in worst case)
- maximum bus latency

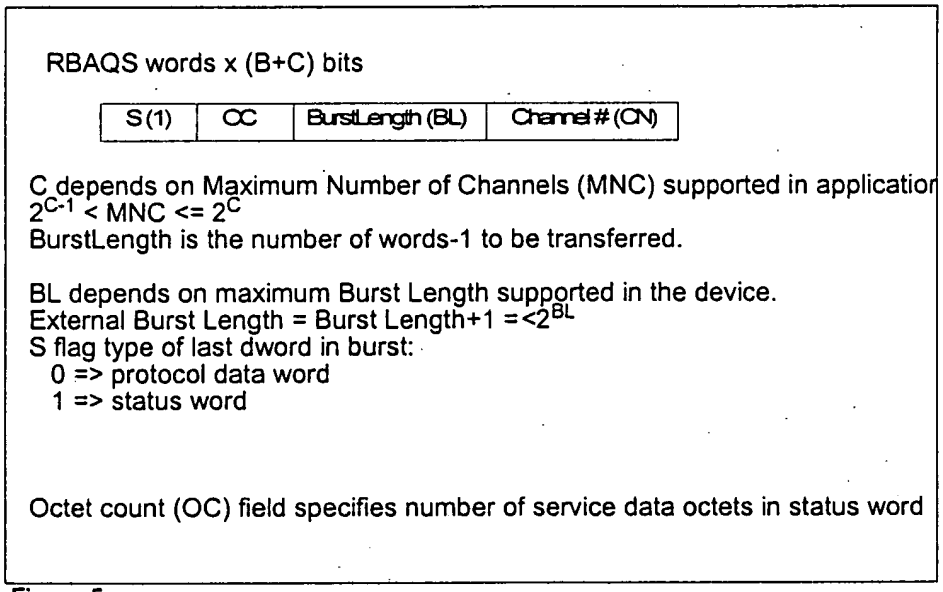

Figure 5
Layout of the RB Action Queue (RBAQ)

The discard of data chains which occurs PMR asserts PRDISCARD during a dword transfer is handled during normal FIFO event processing. The FIFO entry is coded as a non-status event (S=0) but with octet count OC/= 0. Normal data entries write OC=0. When the event is read, the buffer segment is walked but no DMUR bus cycle is executed. Dummy DMUR bus cycles are generated internally so that the sequencers run identically whether a normal DMUR access or discard cycle is running. During this time, the RB does not assert any service request toward the DMUR so that no conflicts will arise between the real and dummy DMUR.

2.2.3.1 Initialization

At reset, all RAMs are automatically initialized. The RB_IIP (Initialization in Progress) flags is asserted active until this is completed and the RB is ready for software initialization. The RBDB data RAM is written with all zeros while the links are chained into the Free Pool (FP). The Free Pool Pointer (FPP) is a register pointing to the start of the chain. A channel buffer is a linked list built from elements taken from this pool.

All RBPT entries are initialized to empty and burst threshold code equal to a default reset value specified in a VHDL package.

The RBAQ (FIFO RAM) is cleared for testing purposes. The FIFO read and write pointer registers are initialized to 0 and the FIFO status set to empty.

2.2.3.2 FIFO service Release of Buffers to Free Pool

FIFO service does not release individual dwords to the RBDB free pool as they are transferred to DMUR. Instead it waits until the last dword of the burst is read. The resulting free buffer chain or segment is released in a single clock by copying the segment start address to the FPP and the old FPP to the link field of the dword at the segment end address. Two auxiliary registers are required to store the beginning and end addresses of the chain being transferred to the DMUR interface:

SEGS = RP (start address of buffer chain segment begin read)

SEGE = RP (end address of buffer chain segment begin read)

2.3 Reset Behavior

2.4 Functional Test Description

2.5 Production Test Description

3 Interfaces and Signal Description

A signal is active high unless "_N" is appended to its name. To make the design as re-usable as possible, a bus signal whose width is application dependent will be specified by one of the following parameters:

Parameter name	Bus Type	Typical value (bits)
CN	Channel Number	8 (256 channels)
DB	Data/Status	32
BT	Burst Threshold Code	4 (max 16 codes)

BL	Burst Length	6 (max burst 64 dw)
OC	Status Service Data Octet Count	2 (0-3 octets)
BA	RB Data Buffer Address	12 (max 4095 dwords)
AQA	Action Queue RAM Address	9 (0 to 512 entries)

3.1 Signal Description

Table 1
Macro Interfaces and Signal Description

Symbol name	I/O	Function
Clock and Reset		
CLK	I	Internal clock (66 MHz)
RESET_N	I	General reset of RB. All registers and RAM reset
STOP	I	Test mode (active high). Stops all channel sequencers.
RB_IIP	O	RB initialization in progress following reset. RB is not available when this signal is asserted. This signal will remain high for 3072 clocks following release of RB reset(s).
Protocol Machine Receive (PMR) Interface		
PRWR_N	I	**Operation Code.** PMR write cycle. Single dword.
PRA[CN-1:0]	I	**Address bus.** Specifies channel number for transfer.
PRD [DB-1:0]	I	**PMR Data/Status** dword being transferred
PRSTAT	I	Mode of data word to be transferred. 0 => protocol data 1 => status + protocol data (0 to 3 octets)
PRSTAT_OC [OC-1:0]	I	Count of data octets in status word being transferred
PRDISCARD	I	Discard open data block for the channel not yet transferred to FIFO.
RB_PRRDY	O	**Ready** End of data transfer indication. 0 => PMR should insert wait state. 1 => RB will finish transfer during this clock cycle.
RB_PRFULL	O	Asserted at end of PMR write cycle (RB_PRRDY=1) to indicate that no additional PMR requests can be accepted due to: • Empty data buffer free pool or • Full FIFO task buffer to the DMUR. De-asserted after DMUR restores free buffers.
Data Management Unit Receive (DMUR) Interface		

Table 1
Macro Interfaces and Signal Description (cont'd)

Symbol name	I/O	Function
DRRD_N	I	DMUR FPI read command. Only single word read transfer is supported but data and address cycles can be overlapped.
DRA	I	1 bit address 0 => status port (channel address, dword count) 1 => data port
RB_DRD[DB-1:0]	O	Output data/status from RB to DMA controller
RB_DRRDY	O	End of data transfer indication. 0 => DMUR should insert wait state. 1 => RB will finish transfer during this clock cycle.
RB_DRSTAT	O	Last word in burst is status
RB_DRREQ_N	O	Service request from RB to DMUR controller. Asserted when RBAQ is not empty.

SMIF Control Interface

BPI_RD_SFR_N[6:1]	I	Read special function registers (select per register) 1 : channel burst length parameter 2 : free pool monitoring mode and interrupt flags 3 : trigger threshold triggers for free pool monitoring 4 : test access command register 5 : test access data register 6 : count of free pool elements (data buffer and fifo)
BPI_WR_SFR_N[5:0]	I	Write special function registers (select per register) 0 : channel command register 1 : channel burst length parameter 2 : free pool monitoring mode and interrupt flags 3 : trigger threshold triggers for free pool monitoring 4 : test access command register 5 : test access data register
BPI_REQ_N	I	Special function register read or write is valid
BPI_DI[DB-1:0]	I	Data input bus
BPI_RDY_N	O	Data cycle ending

Table 1
Macro Interfaces and Signal Description (cont'd)

Symbol name	I/O	Function
BPI_D_O[DB-1:0]	O	Data output bus
Interrupt Interface (IC)		
RB_DBFP_INT	O	RB data buffer free pool threshold interrupt
RB_AQFP_INT	O	RB Action queue free pool threshold interrupt
INT_ACK	I	Interrupt acknowledged
Data Buffer Data/Status RAM Interface (M256F)		
RB_DSR_WN	O	write strobe (active low)
RB_DSR_BSN	O	block select (active low)
RB_DSR_ADR(BA-1:0)	O	address bus
RB_DSR_DI(31:0)	O	write data
RBR_DSR_DO(31:0)	I	read data (output of RB Data Buffer RAM)
Data Buffer Link RAM Interface (M256F)		
RB_DLR_WN	O	write strobe (active low)
RB_DLR_BSN	O	block select (active low)
RB_DLR_ADR(BA-1:0)	O	address bus
RB_DLR_DI(16:0)	O	write data
RBR_DLR_DO(16:0)	I	read data (output of RB Data Link RAM)
Burst Parameter RAM Interface (M256F)		
RB_PTR0_WN	O	write strobe (active low)
RB_PTR0_BSN	O	block select (active low)
RB_PTR0_ADR(CN-1:0)	O	address bus
RB_PTR0_DI(BT-1:0)	O	write data
RBR_PTR0_DO(BT-1:0)	I	read data

Table 1
Macro Interfaces and Signal Description (cont'd)

Symbol name	I/O	Function
Parameter Table RAM Interface (M256F) Parameter Table stores Data buffer read and write pointers, burst threshold code, pre-burst count, and empty flag i.e. PTD=2*BA+BT+BL+1		
RB_PTR1_WN	O	write strobe (active low)
RB_PTR1_BSN	O	block select (active low)
RB_PTR1_ADR(CN-1:0)	O	address bus
RB_PTR1_DI(PTD-1:0)	O	write data
RBR_PTR1_DO(PTD-1:0)	I	read data
Action Queue RAM Interface (M256F) Action Queue Data Bus dimensioned according to channel number, burst length, status flag, and status octet count i.e. AQD = CN+BL+1+OC		
RB_AQR_WN	O	write strobe (active low)
RB_AQR_BSN	O	block select (active low)
RB_AQR_ADR(AQA-1:0)	O	address bus
RB_AQR_DI(AQD-1:0)	O	write data
RBR_AQR_DO(AQD-1:0)	I	read data

3.1.1 RB Interface to the Protocol Machine Receive (PMR)

The PMR initiates data transfer with an address cycle i.e. active write signal PRWR_N and all control data valid (channel address, status flag, octet count, and discard flag). RB will read the PMR's data with 1 wait state and assert RB_PRRDY. PMR can write 1 dword every 3 clock cycles.

The out-of-band signals are:

- PRSTAT to indicate if transferred word is status instead of pure 32-bit data. Captured by RB during address phase.
- PRSTAT_OC to indicate the number of service data octets are contained in the status word when PR_STAT is asserted.
- PRDISCARD to indicate that this dword and any other dwords not transferred to the DMUR FIFO should be discarded.

• RB_PRFULL to stop PMR transfers when the RB has no free buffer space.

The PMR interface does not support overlapped transfers.

The RB_PRFULL signal will be asserted simultaneously with RB_PRRDY. **PMR must not attempt another transfer until this flag is de-asserted.**

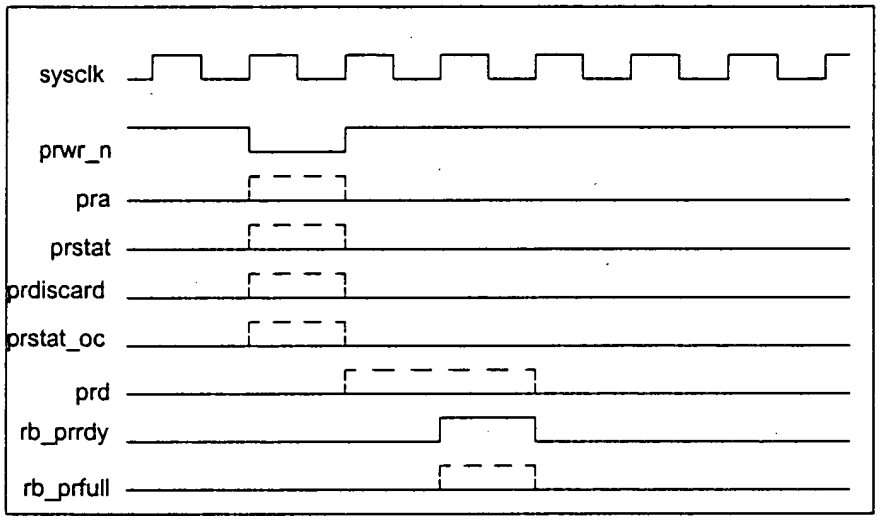

Figure 6
FPI Dword Transfer from PMR to RB

3.1.2 RB Interface to Data Management Unit Receive (DMUR)

The RB interface to the DMUR is similar to a unidirectional FPI slave bus timing. Because of the simple nature of the interface, opcode and select signals are not necessary. DMUR reads a status register when DRA=0 and the FIFO data port when DRA=1.

Two out-of-band signals are required:

1. RB_DRREQ_N to indicate that the FIFO is not empty.

2. RB_DRSTAT to indicate if dword being transferred is status or only data. This signal is asserted only during the last dword of a burst when that dword contains status. The last dword is the only allowed position for a status word in a burst.

DMUR initiates a block transfer by asserting a read request at address 0. During the data phase, RB asserts RB_DRRDY along with the status register shown in Table 2.

Table 2
RB DMUR Status Register

Bit	31...27	26 ...25	24	23..22	21..16	15..8	7..0
		Octet count in status dword	Status flag		Burst length		Ch #

DMUR then transfers "Burst length" + 1 dwords with either individual or overlapped read cycles at word address 1. Transfers are synchronized with the ready signal. Internally the PMR has higher priority and will force additional wait states in the event of conflict. Note that although the DMUR could overlap the first data transfer cycle with the status register read, this may not be useful in practical designs as the DMUR would not know the required burst read length. The current implementation of RB always asserts at least 1 wait state at the beginning of each DMUR read opeation and at least 1 wait state after every 2 words in a burst. Additional wait states are inserted due to PMR access contention (approximately 2 clocks per PMR write access will create contention for longer DMUR burst access N > 4). For single DMUR data transfers, contention increases. There is never contention for status register read.

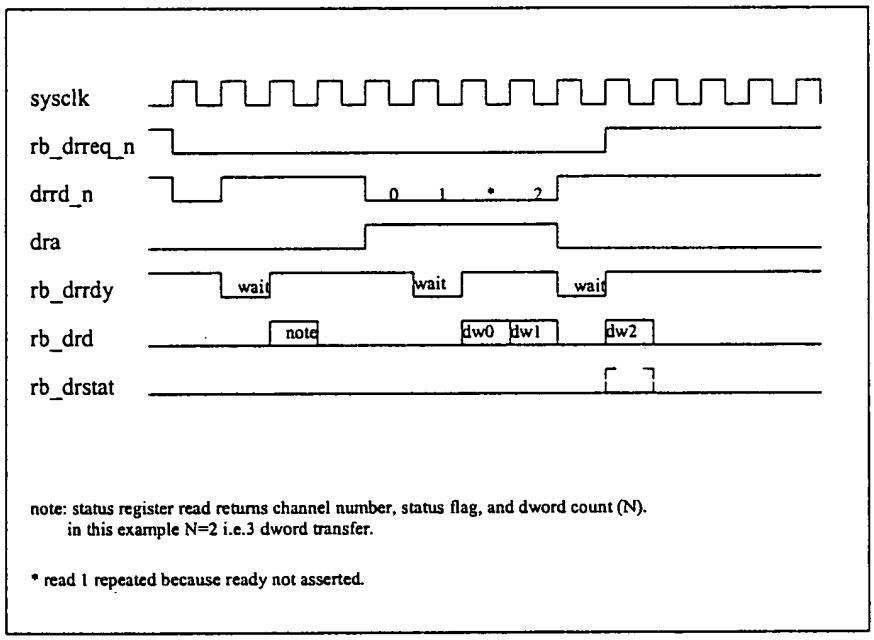

Figure 7
DMUR transfers 3 dwords

3.1.3 RB Control Bus (SMIF)

The SMIF interface provides a set of registers for configuration and testing. Register layouts are specified by package constants for an application and are therefore only funcitonally described here. Refer to the Appendix for an application example.

Addressing of channel specific data and all internal RAM is done using an indirect address register.

SFR R/W index		Description
0	W	Channel Command Register Channel Number: CN bits specify the channel number for the command. Commands (at least 2 bits): The following commands are supported: 1. initialize channel 2. debug (writes channel number only) 3. no operation
1	R/W	Burst Threshold Code BT bits specify a burst code which translates to a burst length in dwords. All definitions of the burst length are specified in the VHDL package.

SFR R/W index		Description
2	R/W	Configuration Register Two flags are provided to configure the Free Pool (FP) Monitor. The bit positions of these flags are specified in the VHDL package. a. Free Pool (FP) Monitor Mode 0 -> capture minimum FP count 1 -> interrupt if FP count falls below threshold programmed in Threshold Register. b. RB FP Interrupt Mask 0 -> enable FP monitor interrupt 1 -> disable FP monitor interrupt
3	R/W	Free Pool Interrupt Threshold Parameters Bits Definition 0 - BA-1 RBDB free pool threshold 16 - 15+AQA RBAQ free pool threshold If free pool mode flag is '0' (minimum pool capture mode), reading this register returns the minimum free pool counts detected since the last read of this register. The read access resets the counts to maximum. If free pool mode is '1' (threshold interrupt mode), reading this register returns the current programmed threshold values.

SFR R/W index		Description
4	R/W	Test Command Register RAM address (BA bits) : RAM address used by access to Test Data Register. Placement of this bit field in the SMIF data bus is set in VHDL package. Its width is assumed to be BA bits which is the largest address range in the RB. Test Commands (at least 3 bits): A command opcode supports RAM testing and set/reset of test mode which forces a buffer full state. Width and placement of this opcode bit field is specified in VHDL package. a. R/W Burst Threshold Parameter RAM b. R/W Parameter Table (channel state) c. R/W Data Buffer RAM d. R/W Link RAM e. R/W Action Queue RAM f. Set test mode g. Reset test mode auto increment mode (1 bit) : following read or write of Test Data Register 0-> no post increment of address register 1-> post increment of address register command validation code : RB accepts command only if code matches constant specified in VHDL package. Width specified by application.

SFR R/W index		Description
5	R/W	Test Data Register. Read or write of this register reads or writes RAM specified in Test Command Register. If auto increment mode is active, the address will be automatically advanced to next word address. The address will wrap around automatically at the end of the selected RAM. Width of data bus depends on addressed RAM. A data is aligned to bit 0 of the SMIF data bus.
6	R	Current Free Pool Count (read only) 0 - BA-1 Data Buffer FP count 16-15+AQA FIFO FP count

A.1 Introduction

The M256F Network Controller uses the RB Macro as a buffer between its protocol machine Receive (PMR) and Data Management Unit Receive (DMUR). The application wraps the RB in a shell for:

- Adaptation of SMIF registers to Slave FPI Bus with daisy chained data bus
- Mapping of RB interrupts to daisy chained interrupt vector bus
- Hardware and Software controlled reset capability

The M256F dimensioning parameters which are specified at synthesis time are:

- 256 channels
- 3072 dword data buffer
- 512 word FIFO (action queue for DMUR read requests)
- 10 burst codes (1, 4, 8, 12, 16, 24, 32, 40, 48, 64)
- Macro ID for test access = "0011"
- 8-bit channel command field: nop="00000000", init="00000001",debug="00010000"

The RB shell structure is shown in Figure 1.

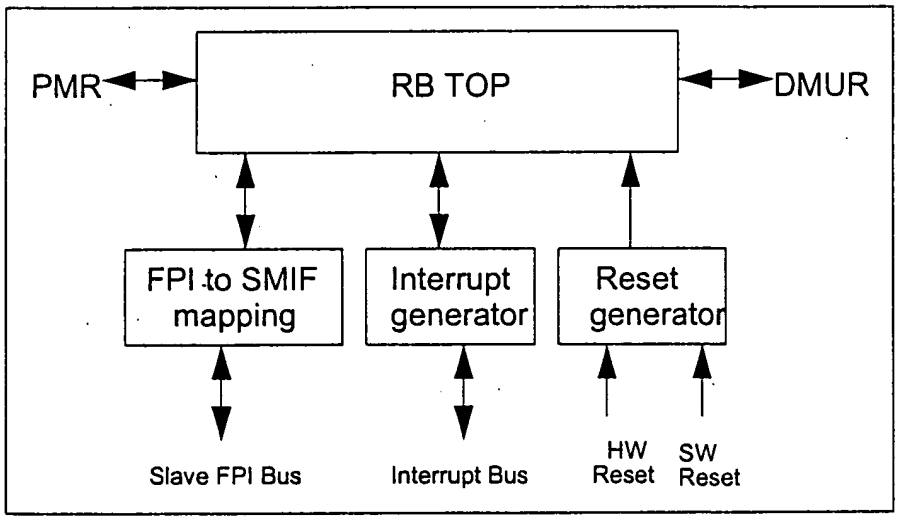

Figure A.1

RB Shell Structure for M256F Application

A.2 RB Dimensioning

A.2.1 Receive Buffer Parameter Table (RBPT)

The RBPT RAM control word for the M256F stores 12 bit addresses for the data buffer (3K words) and supports 10 burst codes (4 bits) with a maximum burst length of 64 (6 bits).

The parameter table is implemented in 2 separately addressable RAMs :

1. 256 x 4 bits for Burst Parameter Code (BC)
2. 256 x 31 bits for (read and write pointers, pre-burst count, and buffer empty flag)

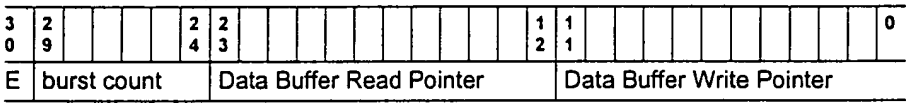

Figure A.2 Bit Assignments in Parameter Table 1 RAM (all but Burst Code)

The E bit is the empty flag. When E=1, the channel has an empty buffer chain and no FIFO Action Queue events.

A.2.2 RB Data Buffer (RBDB)

The M256F data buffer is implemented in 2 physical RAMs:

1. 3072 x 32 bits (dword buffer)
2. 3072 x 12 bits (chain link buffer)

A.2.3 RB Action Queue (RBAQ)

The Action Queue is implemented in a 512 word x 17 bit RAM. The status flag S and Octet Count OC are fixed for all 32 bit applications. The Burst Length and channel number are application specific.

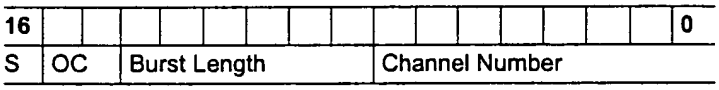

Figure A.3 Bit Assignments in Action Queue RAM

Note that if S=0 and OC /= 0, the event is a discard event i.e. RB will read the data buffer chain of "Burst Length" dwords but not report them to the DMUR.

A.3 M256F RB Shell Signals

Table A.3
RB Interfaces and Signal Descriptions for M256F

Symbol name	I/O	Function
Clock and Reset		
SYSCLK	I	Internal clock (66 MHz maximum)
HW_RESET_N	I	General reset of RB. All registers and RAM reset Unclocked assert, de-assert synchronous to SYSCLK
SW_RESET_N	I	General reset of RB. All registers and RAM reset Assert and de-assert synchronous to SYSCLK
GC_STOP	I	Test mode (active high). Stops all channel sequencers.
RB_IIP	O	RB initialization in progress following reset. RB is not available when this signal is asserted. This signal will remain high for 3072 clocks following release of RB reset(s).
Protocol Machine Receive (PMR) Interface		
PR_RB_WR_N	I	**Operation Code.** PMR write cycle. Single dword.
PR_RB_A[7:0]	I	**Address bus.** Specifies channel number for transfer.
PR_RB_D [31:0]	I	**PMR Data/Status** dword being transferred
RB_PR_RDY	O	**Ready** End of data transfer indication. 0 => PMR should insert wait state. 1 => RB will finish transfer during this clock cycle.
PR_RB_STAT	I	Mode of data word to be transferred. 0 => protocol data 1 => status + protocol data
PR_RB_DISCARD	I	Discard data not yet written to Action Queue. only evaluated if PR_RB_STAT=1. 0 => no discard 1 => discard
PR_RB_STAT_OC [1:0]	I	Count of data octets in status word being transferred

Table A.3
RB Interfaces and Signal Descriptions for M256F

Symbol name	I/O	Function
RB_PR_FULL	O	Asserted at end of PMR write cycle if: • Buffer free pool becomes empty or • FIFO task buffer to the DMA channel becomes full. De-asserted after DMA read cycle.

Data Management Unit Receive (DMUR) Interface

DR_RB_RD_N	I	DMUR FPI read command. Only single word read transfer is supported but can be overlapped.
DR_RB_A	I	select status or data port 0 => read status register (block size, channel number) 1 => data port (data or status dword)
RB_DRD[31:0]	O	Output data/status from RB to DMA controller
RB_DR_RDY	O	End of dword transfer 0 => DMUR should insert wait state. 1 => RB will finish transfer during this clock cycle.
RB_DR_STAT	O	Current dword is status type
RB_DR_REQ_N	O	Service request from RB to DMUR controller. Asserted when data available for transfer(burst threshold reached or status dword received from PMR).

Target FPI Slave Interface

PB_TFPI_A[8:2]	I	Address bus.
PB_TFPI_D[31:0]	I	Input data bus.
PB_TFPI_WR_N PB_TFPI_RD_N	I I	Read/Write controls. Following codes are defined: WR_N = 1; RD_N = 1 => NOP WR_N = 0; RD_N = 1 => data written to DMUR WR_N = 1; RD_N = 0 => data read from DMUR
PB_TFPI_RDY_EN	I	Enable start of bus cycle
PB_VC_TFPI_SEL_N	I	Select virtual channel registers block
PB_VG_TFPI_SEL_N	I	Select virtual global registers block
PB_RB_TFPI_SEL_N	I	Select RB specific registers block

Table A.3
RB Interfaces and Signal Descriptions for M256F

Symbol name	I/O	Function
RB_TFPI_RDY	O	Data cycle ending
RB_TFPI_D[31:0]	O	Output data bus.
Interrupt Controller Interface (IC)		
RB_IC_REQ_N	O	RB Interrupt Active
IC_RB_GNT_N	I	Interrupt acknowledged
IC_D[31:0]	I	Interrupt vector from macro in daisy chain
RB_IC_D[31:0]	O	Interrupt vector output next macro or interrupt controller
Data Buffer Data/Status RAM Interface (M256F)		
RB_DSR_WN	O	write strobe (active low)
RB_DSR_BSN	O	block select (active low)
RB_DSR_E(11:0)	O	address bus
RB_DSR_ED(31:0)	O	write data to ram
RBR_DSR_AZ(31:0)	I	read data from ram
Data Buffer Link RAM Interface (M256F)		
RB_DLR_WN	O	write strobe (active low)
RB_DLR_BSN	O	block select (active low)
RB_DLR_E(11:0)	O	address bus
RB_DLR_ED(16:0)	O	write data to ram
RBR_DLR_AZ(16:0)	I	read data from ram
Burst Parameter RAM Interface (M256F)		
RB_PTR0_WN	O	write strobe (active low)
RB_PTR0_BSN	O	block select (active low)
RB_PTR0_E(7:0)	O	address bus
RB_PTR0_ED(3:0)	O	write data to ram
RBR_PTR0_AZ(3:0)	I	read data from ram

Table A.3
RB Interfaces and Signal Descriptions for M256F

Symbol name	I/O	Function
Parameter Table RAM Interface		
RB_PTR1_WN	O	write strobe (active low)
RB_PTR1_BSN	O	block select (active low)
RB_PTR1_E(7:0)	O	address bus
RB_PTR1_ED(30:0)	O	write data
RBR_PTR1_AZ(30:0)	I	read data
Action Queue RAM Interface		
RB_AQR_WN	O	write strobe (active low)
RB_AQR_BSN	O	block select (active low)
RB_AQR_E(8:0)	O	address bus
RB_AQR_ED(16:0)	O	write data to ram
RBR_AQR_AZ(16:0)	I	read data from ram

A.4 Reset Adaptation

The M256F requires both a hardware and software controlled resets. A project specific macro reset block is provided which combines these resets into a single reset for the RB top level and is transparent to the RB core.

A.5 Interrupt Adaptation

The M256F maps the RB interrupts into a 32 bit vector that is combined with interrupt vectors from other macros in a daisy chained bus. A macro's interrupt vector output becomes the interrupt vector input of the next macro in the chain. That macro forms its output by the bit-by-bit 'or' of its interrupt vector with the input interrupt vector. A macro must hold its interrupt vector to all zeros until it is granted the bus to avoid disturbing other macros which may be using the bus.

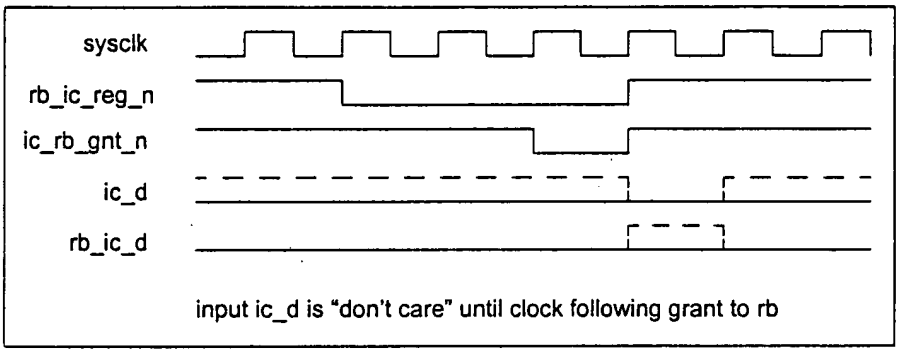

Figure A.4 RB Interrupt Bus Request/Grant Sequence

31															16
1	1	1	0	0	Queue ID(0-7)			0	0	0	0	0	RBI	AQI	0

15															0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure A.5 RB Interrupt Vector for generated for M256F application

A.6 FPI Adaptation to SMIF

The M256F uses 32 bit variant of the FPI bus. The bus is simplified and supports only overlapped read or write cycles.

The TFPI bus registers specify channel configuration and support TB testing. Addressing of channel specific data and all internal RAM is done using an indirect addressing scheme to minimize the required address space.

All addresses are dword aligned. Note that the address bus does support octet addressing (bits 0 and 1 are not implemented and are set to '0' internally).

The data output bus is a daisy chained bus (refer to previous section for basic concept). When the RB is not being addressed, it keeps its output data contribution to the daisy chain at all zeros so that it does not disturb other bus users.

RB Application : M256F

A concept used in the M256F is the virtual register. The concept was developed to allow certain data which is distributed over more than 1 macro to be viewed by external software as single register. This hides internal macro function split from the user at the top level because such structure is a convenience for the chip developer and not of interest to the user. Internally, the FPI bus interface decodes certain address ranges corresponding to these virtual data blocks. Three select signals are generated for RB:

1. Virtual Channel register select (PB_VC_TFPI_SEL_N). Data in the block is channel specific and is distributed over all macros handling protocol channels. RB receives small slice of channel data (burst threshold parameter) which is captures on write of a specific row address of channel data. It returns this small slice on any read of the virtual register row address containing the parameter.
2. Virtual Global register select (PB_VG_TFPI_SEL_N). Data in this block is also distributed over multiple macros but is not channel specific. This data group includes system interrupt queue ID, masks for its interrupts, free pool monitoring modes, and test command for RB. The test command register uses another level of addressing via a macro id field. When the register is written with a valid macro id, the ownership of the test command and test data register passes to that id. The RB is assigned "0011" for M256F.
3. RB specific register select (PB_RB_TFPI_SEL_N). These are registers exclusive to the RB such as free pool counters.

The RB will not start FPI cycle until the input ready PB_TFPI_RDY is asserted. Once a bus cycle begins, it will extend its read ready cycle i.e. drive its output data bus until the input PB_TFPI_RDY goes high. This signal is the AND of all macro ready signals and stretches a virtual register read until the slowest macro data is available.

Table A.4 FPI Addresses for M256F Registers

Address Offset		Register Description
00 Hex PB_VC_TFPI_SEL_N must be asserted	W	Virtual Channel Register Command bits 0 - 7 : channel number 16 - 23 : command The following commands are supported: 1: initialize channel (accept burst parameter) 5: debug (writes channel number only) 6: no operation All other commands ignored.
20 Hex PB_VC_TFPI_SEL_N must be asserted	R/W	Virtual Channel Bus Burst Length bits 0-3 are burst parameter code: code dword burst length 0 1 1 4 2 8 3 12 4 16 5 24 6 32 7 40 8 48 9 64 10-15 are mapped to burst length 64

Address Offset		Register Description
40 Hex PB_VG_TFPI_SEL_N must be asserted	R/W	Configuration1: bit 2: Free Pool Monitor Mode 0 -> capture minimum free pool count 1 -> interrupt if free pool falls below threshold programmed in RB Threshold Register. Reset value is '0'. bit 5: RB Interrupt Mask 0 -> enable free pool monitor interrupt 1 -> disable free pool monitor interrupt Reset value is '0'.
44 Hex PB_VG_TFPI_SEL_N must be asserted	W	Configuration 2 bits 28-30: System Interrupt Queue ID RB sends free pool monitoring interrupts to this queue.
58 Hex Only valid if TFPI_SEL_VG_N is asserted	W	Test Command Register bits 0-11 : address field bits 16-23 : Command 0 - R/W Burst Threshold Parameter RAM 1 - R/W Parameter Table (except BTC) 2 - R/W Data Buffer RAM 3 - R/W Link RAM 4 - R/W Action Queue RAM 5 - Set test mode (manufacturing test) 6 - Reset test mode bit 24: auto increment mode following read or write of Test Data Register 0-> no post increment of address register 1-> post increment of address register bits 28-31: target address verification code. RB accepts command if code="0011"

Address Offset		Register Description
5C Hex PB_VG_TFPI_SEL_N must be asserted	R/W	Test Data Register. Read or write of this register reads or writes RAM specified in previous Test Command Register. If auto increment mode is active, address will be automatically advanced to next word address after access. Address wraps automatically at end of selected RAM. Width of data bus depends on command written to command register: 0 - 4 bits 1 - 31 bits 2 - 32 bits 3 - 12 bits 4 - 17 bits 5 - data register not used 6 - data register not used
B0 hex PB_RB_TFPI_SEL_N must be asserted	R	Free Pool Counters (read only) bits 0-11: current free data pool data count bits 12-15: reserved (set to zero) bits 16-23: free action queue free pool count bits 24-31: reserved (set to zero)
B4 hex PB_VC_TFPI_SEL_N must be asserted	R/W	Free Pool Interrupt Threshold Parameters bits 0-11: data buffer free pool threshold bits 12-15: reserved (set to zero) bits 16-23: action queue free pool threshold bits 24-31: reserved (set to zero) If free pool mode is "minimum pool capture", reading this register returns the minimum free pool counts observed since the last read. A read resets the counts to maximum. If free pool mode is "threshold interrupt", reading this register returns the current programmed threshold values.

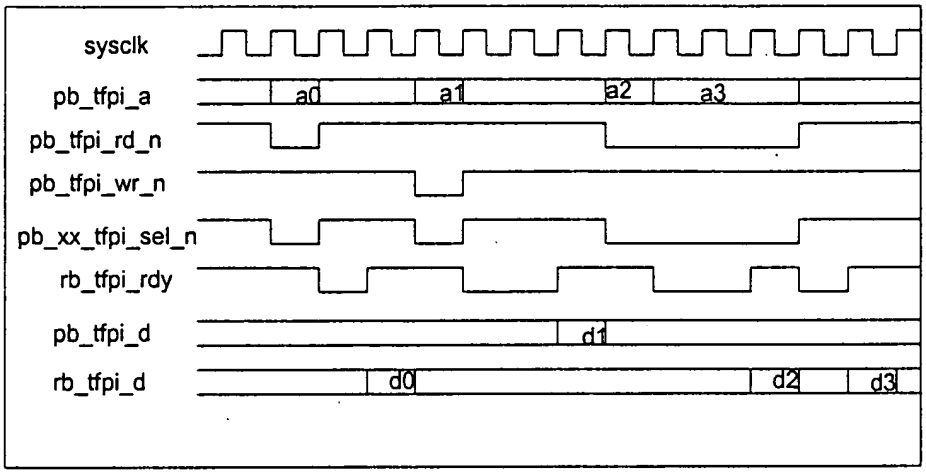

Figure A.6 FPI bus cycles : 1 read + 1 write + 2 overlapped reads